AMENDMENTS TO THE CLAIMS

1. (original): An analog to digital (A/D) converter, comprising:

a counter circuit for storing a digital word;

a ramp generator for generating a sequence of reference voltages which vary in accordance with at least a first transfer function of said digital word and a second transfer function of said digital word;

a comparator for comparing the magnitude of one of said reference voltages with a magnitude of an input signal; and

a control circuit for determining the digital word corresponding to the input signal by repeatedly:

comparing the magnitude of the input signal with the magnitude of a most recently generated reference voltage of said sequence,

incrementing said counter, and

causing said ramp generator to generate a new one of said sequence

until the magnitude of the most recently generated reference voltage of said sequence exceeds the magnitude of said input signal.

2. (original): The converter of claim 1, wherein said first transfer function maps each digital word stored in said counter below a first threshold to a corresponding reference signal in a linear manner.

3. (original): The converter of claim 2, wherein said second transfer function maps a set of non-sequential and increasing digital words stored in said counter each having a magnitude at least equal to said first threshold to corresponding reference signals in a linear manner.

4. (original): The converter of claim 2, wherein said second transfer function maps each increasing digital word stored in said counter having a magnitude at least equal to said first threshold to corresponding reference signals in a logarithmic manner.

5. (original): The converter of claim 1, wherein said counter circuit comprises:

a controller for receiving a reset signal and a clock signal;

a register, coupled to said controller; and

a memory, coupled to said controller,

wherein:

when a clock signal is supplied to said controller, said controller reads a next value from said memory and stores said next value in said register; and

said memory stores a plurality of numbers in a non-sequential and increasing manner.

6. (original): The converter of claim 5, wherein said memory is a non-volatile memory.

7. (original): The converter of claim 1, wherein said counter circuit comprises:

a counter; and

circuitry for incrementing said digital word stored in said counter by one.

8. (original): The converter of claim 1, wherein said ramp generator comprises:

a plurality of capacitor banks, each bank comprising:

a plurality of capacitors having equal capacitance;

a bank output line coupled to a first plate of each capacitor; and

a bank control circuit, coupled to a second plate of each capacitor, and for switchably coupling the second plate of any one of said capacitors to either a first voltage source or a second voltage source;

a master output line, coupled to each bank output line; and

a master controller, for sending control signal to each bank control circuit to a master voltage at said master output line to generate said sequence of voltages.

9. (original): The converter of claim 8, wherein a capacitance of any capacitor in a first capacitor bank is different from a capacitance of any capacitor in a second capacitor bank.

10. (original): The converter of claim 8, wherein the capacitance of any capacitor in a first capacitor bank is a power of 2 of a capacitance of any capacitor in a second capacitor bank.

11. (original): A imaging system, comprising:

a pixel array;

a sample and hold circuit, coupled to said pixel array;

a driver, coupled to said sample and hold circuit;

an analog to digital (A/D) converter, coupled to said sample and hold circuit, said A/D converter comprising:

a counter circuit for storing a digital word;

a ramp generator for generating a sequence of reference voltages which vary in accordance with at least a first transfer function of said digital word and a second transfer function of said digital word;

a comparator for comparing the magnitude of one of said reference voltages with a magnitude of an input signal; and

a control circuit for determining the digital word corresponding to the input signal by repeatedly:

comparing the magnitude of the input signal with the magnitude of a most recently generated reference voltage of said sequence,

incrementing said counter, and

causing said ramp generator to generate a new one of said sequence,

until the magnitude of the most recently generated reference voltage of said sequence exceeds the magnitude of said input signal;

a digital processing circuit, coupled said A/D converter;

a storage circuit, coupled to said digital processing circuit; and

a control circuit, coupled to said pixel array, sample and hold circuit, driver, A/D converter, digital processing circuit, and storage circuit.

12. (original): The imaging system of claim 11, wherein said first transfer function maps each digital word stored in said counter below said first threshold to a corresponding reference signal in a linear manner.

13. (original): The imaging system of claim 12, wherein said second transfer function maps a set of non-sequential and increasing digital words stored in said counter each having a magnitude at least equal to said first threshold to corresponding reference signals in a linear manner.

14. (original): The imaging system of claim 12, wherein said second transfer function maps each increasing digital word stored in said counter having a magnitude at least equal to said first threshold to corresponding reference signals in a logarithmic manner.

15. (original): The imaging system of claim 11, wherein said counter circuit comprises:

a controller for receiving a reset signal and a clock signal;

a register, coupled to said controller; and

a memory, coupled to said controller;

wherein:

when a clock signal is supplied to said controller, said controller reads a next value from said memory and stores said next value in said register; and

said memory stores a plurality of numbers in a non-sequential and increasing manner.

16. (original): The imaging system of claim 15, wherein said memory is a non-volatile memory.

17. (original): The imaging system of claim 11, wherein said counter circuit comprises:

a counter; and

circuitry for incrementing said digital word stored in said counter by one.

18. (original): The imaging system of claim 11, wherein said ramp generator comprises:

a plurality of capacitor banks, each bank comprising:

a plurality of capacitors having equal capacitance;

a bank output line, coupled to a first plate of each capacitor; and

a bank control circuit, coupled to a second plate of each capacitor, and for switchably coupling the second plate of any one of said capacitors to either a first voltage source or a second voltage source;

a master output line, coupled to each bank output line; and

a master controller, for sending control signal to each bank control circuit to a master voltage at said master output line to generate said sequence of voltages.

19. (original): The imaging system of claim 18, wherein a capacitance of any capacitor in a first capacitor bank is different from a capacitance of any capacitor in a second capacitor bank.

20. (original): The imaging system of claim 18, wherein the capacitance of any capacitor in a first capacitor bank is a power of 2 of a capacitance of any capacitor in a second capacitor bank.

21. (original): A processor based system, comprising:

a bus;

a processor coupled to said bus;

a imaging subsystem, coupled to said bus;

wherein said imaging subsystem comprises:

a pixel array;

a sample and hold circuit, coupled to said pixel array;

a driver, coupled to said sample and hold circuit;

an analog to digital (A/D) converter, coupled to said sample and hold circuit, said A/D converter comprising:

a counter circuit for storing a digital word;

a ramp generator for generating a sequence of reference voltages which vary in accordance with at least a first transfer function of said digital word and a second transfer function of said digital word;

a comparator for comparing the magnitude of one of said reference voltages with a magnitude of an input signal; and

a first control circuit for determining the digital word corresponding to the input signal by repeatedly

comparing the magnitude of the input signal with the magnitude of a most recently generated reference voltage of said sequence,

incrementing said counter, and

causing said ramp generator to generate a new one of said sequence, until the magnitude of the most recently generated reference voltage of said sequence exceeds the magnitude of said input signal;

a digital processing circuit, coupled said A/D converter;

a storage circuit, coupled to said digital processing circuit; and

a second control circuit, coupled to said pixel array, sample and hold circuit, driver, A/D converter, digital processing circuit, and storage circuit.

22. (original): The system of claim 21, wherein said first transfer function maps each digital word stored in said counter below said first threshold to a corresponding reference signal in a linear manner.

23. (original): The system of claim 22, wherein said second transfer function maps a set of non-sequential and increasing digital words stored in said counter each having a magnitude at least equal to said first threshold to corresponding reference signals in a linear manner.

24. (original): The system of claim 22, wherein said second transfer function maps each increasing digital word stored in said counter having a magnitude at least equal to said first threshold to corresponding reference signals in a logarithmic manner.

25. (original): The system of claim 21, wherein said counter circuit comprises:

a controller for receiving a reset signal and a clock signal;

a register, coupled to said controller; and

a memory, coupled to said controller;

wherein:

when a clock signal is supplied to said controller, said controller reads a next value from said memory and stores said next value in said register; and

said memory stores a plurality of number in a non-sequential and increasing manner.

26. (original): The system of claim 25, wherein said memory is a non-volatile memory.

27. (original): The system of claim 21, wherein said counter circuit comprises:

a counter; and

circuitry for incrementing said digital word stored in said counter by one.

28. (original): The system of claim 21, wherein said ramp generator comprises:

a plurality of capacitor banks, each bank comprising:

a plurality of capacitors having equal capacitance;

a bank output line, coupled to a first plate of each capacitor; and

a bank control circuit, coupled to a second plate of each capacitor, and for switchably coupling the second plate of any one of said capacitors to either a first voltage source or a second voltage source;

a master output line, coupled to each bank output line; and

a master controller, for sending control signal to each bank control circuit to a master voltage at said master output line to generate said sequence of voltages.

29. (original): The system of claim 28, wherein a capacitance of any capacitor in a first capacitor bank is different from a capacitance of any capacitor in a second capacitor bank.

30. (original): The system of claim 28, wherein the capacitance of any capacitor in a first capacitor bank is a power of 2 of a capacitance of any capacitor in a second capacitor bank.

31. (currently amended): A method for converting an analog signal to a digital word, comprising:

measuring a magnitude of said analog signal;

if said magnitude is not greater than a predetermined ~~first~~ threshold, mapping said magnitude to a digital word in accordance with a first transfer function; and

if said magnitude is at least equal to said predetermined ~~first~~ threshold, mapping said magnitude to the digital word in accordance with a second transfer function.

32. (currently amended): The method of claim 31, wherein said first transfer function maps each magnitude below said predetermined ~~first~~ threshold to a corresponding reference signal in a linear manner.

33. (currently amended): The method of claim 32, wherein said second transfer function maps a set of non-sequential and increasing magnitudes each at least equal to said predetermined ~~first~~ threshold to corresponding reference signals in a linear manner.

34. (currently amended): The method of claim 32, wherein said second transfer function maps each magnitude at least equal to said predetermined ~~first~~ threshold to corresponding reference signals in a logarithmic manner.

35. (canceled):

36. (currently amended): A method for operating an imaging system, comprising:

receiving an analog pixel signal from a pixel;

converting said analog pixel signal into a digital word, wherein said converting comprises:

measuring a magnitude of said analog signal;

if said magnitude is not greater than a predetermined ~~first~~ threshold, mapping said magnitude to a digital word in accordance with a first transfer function; and

if said magnitude is at least equal to said predetermined ~~first~~ threshold, mapping said magnitude to the digital word in accordance with a second transfer function.

37. (currently amended): The method of claim 36, wherein said first transfer function maps each magnitude below said predetermined ~~first~~ threshold to a corresponding reference signal in a linear manner.

38. (currently amended): The method of claim 37, wherein said second transfer function maps a set of non-sequential and increasing magnitudes each at least equal to said predetermined ~~first~~ threshold to corresponding reference signals in a linear manner.

39. (currently amended): The method of claim 37, wherein said second transfer function maps each magnitude at least equal to said predetermined ~~first~~ threshold to corresponding reference signals in a logarithmic manner.

40 - 43. (canceled):

44. (currently amended): An ~~The~~ imaging system comprising: ~~of claim 43,~~

a pixel array;

an analog to digital (A/D) converter circuit that receives analog signals from the pixel array and converts the analog signals to digital signals with a variable level of quantization, said A/D converter circuit comprising,

a linear A/D converter, for producing intermediate values from said analog signals, and

a processing circuit that remaps value said intermediate values produced by said linear A/D converter using

~~wherein said processing circuit remaps values by consulting~~ a mapping table.

45. (canceled):

46 – 47. (canceled):